This application is submitted in the name of inventor Sinan Kaptanoglu, Assignor to Actel Corporation, a California Corporation.

updated

SPECIFICATION

BLOCK CONNECTOR SPLITTING IN LOGIC BLOCK OF A FIELD PROGRAMMABLE GATE ARRAY

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of co-pending United States Patent Application Serial Number 09/880,679, filed June 12, 2001, which is now a U.S Patent 6,624,657, which is a continuation of United States Patent Application Serial Number 09/518,973, filed March 6, 2000, now issued as United States Patent Number 6,285,212.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to a field programmable gate array (FPGA) architecture. More particularly, the present invention relates to the routing resources within a logic block for increasing the routing flexibility in an FPGA architecture.